Amendments to the Specification:

Please replace the first full paragraph on page 5 with the following amended paragraph:

As will be described in more detail below, one embodiment includes a system including a pipeline microprocessor for out-of-order processing of predicated instructions ~~is disclosed~~. The microprocessor includes multiple dynamic pipeline stages including at least one predicated instruction wherein the predicated instruction includes at least one guarding predicate. The microprocessor also includes a register renaming unit, a reorder buffer, multiple execution units and multiple reservation stations. The register renaming unit, the reorder buffer, the plurality of execution units and the plurality of reservation stations are coupled to at least one of the dynamic pipeline stages. The microprocessor also includes an augmented register alias table. Also disclosed is a method of operating a microprocessor for out-of-order processing of predicated instructions.

Please replace the paragraph bridging pages 8 and 9 with the following amended paragraph:

Fig. 2 illustrates where the instructions may have traveled in the pipeline [[200]]. In Fig. 2, the add instructions have already advanced down the pipeline. As mentioned before, if predicates p9 and p3 have not yet been resolved, the mov instruction must wait indefinitely before the entering rename stage 210. After the predicates p9 and p3 become resolved, the mov instruction can then advance down the pipeline [[200]] into the rename stage 210 to rename the mov instruction source operand to rB or rC.